IN THE CLAIMS

1. (Canceled)

2. (Currently Amended) ~~The~~ A capacitor ~~according to claim 1~~ , comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode;

a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and one of the first and second electrodes; and

wherein the one electrode is a tungsten nitride and the buffer layer is a tungsten oxide.

3. (Original) The capacitor according to claim 2, wherein the dielectric layer is a tantalum oxide.

4. (Currently Amended) ~~The~~ A capacitor ~~according to claim 1~~ , comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode;

a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and one of the first and second electrodes; and

wherein the buffer layer has a orthorhomic crystalline structure.

5. (Previously Presented) A capacitor, comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

a tungsten trioxide buffer layer interposed between and directly adjoining the dielectric layer and one of the first and second electrodes.

6. (Original) The capacitor according to claim 5, wherein the buffer layer has a orthorhomic crystalline structure.

7. (Original) The capacitor according to claim 5, wherein the one electrode includes tungsten.

8. (Original) The capacitor according to claim 7, wherein the buffer layer is grown by oxidizing the one electrode.

9. (Previously Presented) A capacitor, comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer interposed between and directly adjoining the dielectric layer and one of the first and second electrodes, wherein the metal oxide buffer layer includes a refractory metal.

10. (Original) The capacitor according to claim 9, wherein the buffer layer is of the formula MOx, and M is a metal component from a group consisting of tungsten, tantalum, zirconium, and hafnium.

11. (Original) The capacitor according to claim 9, wherein the buffer layer has a orthorhomic crystalline structure.

12. (Canceled)

13. (Currently Amended) ~~The~~ A vertical capacitor ~~according to claim 12~~ , comprising:

a bottom electrode;

a top electrode positioned above the bottom electrode;

a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and

a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and the bottom electrode, wherein the bottom electrode is a tungsten nitride and the buffer layer is a tungsten oxide.

14. (Original) The capacitor according to claim 13, wherein the dielectric layer is a tantalum oxide.

15. (Currently Amended) ~~The~~ A vertical capacitor ~~according to claim 12~~ , comprising:

a bottom electrode;

a top electrode positioned above the bottom electrode;

a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and

a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and the bottom electrode, wherein the buffer layer has a orthorhomic crystalline structure.

16. (Previously Presented) A capacitor, comprising:

a bottom electrode;

a top electrode;

a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and

a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and the bottom electrode, wherein the metal in the buffer layer is a refractory metal.

17. (Original) The capacitor according to claim 16, wherein the metal in the buffer layer is tungsten.

18. (Original) The capacitor according to claim 17, wherein the bottom electrode comprises a metal nitride, and the metal in the bottom electrode is a refractory metal.

19. (Original) The capacitor according to claim 18, wherein the bottom electrode comprises tungsten nitride.

20. (Previously Presented) A capacitor, comprising:

a bottom electrode;

a top electrode;

a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and

a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and the bottom electrode, wherein the bottom electrode comprises a metal nitride having a metal component which is the same as the metal component of the metal oxide buffer layer.

21. (Original) The capacitor according to claim 20, wherein the dielectric layer comprises tantalum oxide.

22. (Original) The capacitor according to claim 21, wherein the metal component of the bottom electrode and the buffer layer includes tungsten.

23. (Previously Presented) A capacitor, comprising:

a bottom electrode;

a top electrode;

a single compound, dielectric layer interposed between the bottom electrode and the top electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the bottom electrode and the top electrode;

wherein at least one electrode selected from the group consisting of the bottom electrode and the top electrode comprises tungsten nitride.

24. (Original) The capacitor according to claim 23, wherein the dielectric layer is a metal oxide of a different type than the buffer layer.

25. (Previously Presented) A capacitor, comprising:

a first electrode;

a second electrode;

a single compound, tantalum oxide dielectric layer interposed between the bottom electrode and the top electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the bottom electrode and the top electrode;

wherein at least one electrode is selected from the group consisting of the bottom electrode and the top electrode includes tungsten nitride.

26. (Previously Presented) A capacitor, comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and one of the first and second electrodes, wherein the metal oxide buffer layer has an orthorhombic crystal structure.

27. (Original) The capacitor according to claim 26, wherein the metal in the buffer layer is tungsten.

28. (Canceled)

29. (Currently Amended) The capacitor according to claim ~~28~~ 16, wherein the bottom electrode comprises a metal nitride and has a metal component which is the same as the metal component of the metal oxide buffer layer.

30. (Previously Presented) A capacitor, comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and one of the first and second electrodes;

wherein the buffer layer has a dielectric constant greater than the dielectric layer.

31. (Original) The capacitor according to claim 30, wherein the one of the first and second electrodes has a metal component which is the same as the metal component of the buffer layer.

32. (Original) The capacitor according to claim 30, wherein the buffer layer has an orthorhomic crystalline structure.

33-72. (Canceled)

73. (Canceled)

74. (Previously Presented) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode.

75. (Previously Presented) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

wherein at least one electrode selected from the group consisting of the first electrode and the second electrode comprises tungsten nitride.

76. (Previously Presented) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a tungsten nitride second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

a tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and the second electrode.

77. (Previously Presented) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a tungsten nitride second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

a high temperature annealed, tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and the second electrode.

78. (Original) The semiconductor die according to claim 77, wherein the high temperature annealed buffer layer is annealed at least 700 degrees Celsius and has an orthorhomic crystal structure.

79. (Previously Presented) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer is interposed between and directly adjoining the dielectric layer and the second electrode, wherein the buffer layer has an orthorhombic crystal lattice structure.

80. (Previously Presented) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer is interposed between and directly adjoining the dielectric layer and the second electrode,

wherein the buffer layer has a dielectric constant greater than the dielectric layer.

81. (Canceled)

82. (Currently Amended) The memory device according to claim ~~81~~ 80, wherein the electrode selected from the group consisting of the first electrode and the second electrode has a metal component that is the same as the metal component of the buffer layer.

83. (Previously Presented) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

84. (Previously Presented) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, wherein at least one electrode selected from the group consisting of the bottom electrode of the capacitor and the top electrode of the capacitor comprises tungsten nitride;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

85. (Previously Presented) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having an orthorhomibic crystalline structure;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

86. (Previously Presented) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having a dielectric constant greater than the dielectric layer;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

87. (Canceled)

88. (Canceled)

89. (Currently Amended) The module according to claim ~~88~~ 92, wherein the electrode selected from the group consisting of the first electrode and the second electrode includes a metal component that is the same as the metal component of the buffer layer.

90. (Previously Presented) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

91. (Previously Presented) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having a dielectric constant greater than the dielectric layer;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit wherein at least one electrode selected from the group consisting of the bottom electrode of the capacitor and the top electrode of the capacitor comprises tungsten nitride.

92. (Previously Presented) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having an orthorhombic crystalline structure;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

93. (Canceled)

94. (Canceled)

95. (Currently Amended) The system according to claim ~~94~~ 97, wherein the electrode selected from the group consisting of the first electrode and the second electrode includes a metal component that is the same as the metal component of the buffer layer.

96. (Previously Presented) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

97. (Previously Presented) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having an orthorhombic crystalline structure;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

98. (Previously Presented) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having a dielectric constant greater than the dielectric layer;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

99. (Canceled)

100. (Canceled)

101. (Currently Amended) The system according to claim ~~100~~ 103, wherein the electrode selected from the group consisting of the first electrode and the second electrode includes a metal component that is the same as the metal component of the buffer layer.

102. (Previously Presented) An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode.

103. (Previously Presented) An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the bottom electrode and the top electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

wherein the metal oxide buffer layer has an orthorhombic crystalline structure.

104. (Previously Presented) An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the bottom electrode and the top electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

wherein the metal oxide buffer layer has a dielectric constant greater than the dielectric constant of the dielectric layer.

105. (Canceled)

106. (Previously Presented) A capacitor, comprising:

an annealed bottom electrode;

a top electrode;

a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and

an annealed metal oxide buffer layer intermediate and directly adjoining the dielectric layer and the bottom electrode.

107-109. (Canceled)

110. (Canceled)

111. (Currently Amended) ~~The~~ A memory cell ~~according to claim 110,~~ comprising a capacitor and an access device, wherein the capacitor includes:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode;

a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and one of the first and second electrodes; and

wherein the one electrode is a tungsten nitride and the buffer layer is a tungsten oxide.

112. (Currently Amended) ~~The~~ A memory cell ~~according to claim 110,~~ comprising a capacitor and an access device, wherein the capacitor includes:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode;

a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and one of the first and second electrodes; and

wherein the buffer layer has a orthorhombic crystalline structure.

113. (Previously Presented) A memory cell comprising a capacitor and an access device, wherein the capacitor includes:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a tungsten trioxide buffer layer interposed between and directly adjoining the dielectric layer and one of the first and second electrodes.

114. (Original) The memory cell according to claim 113, wherein the one electrode includes tungsten.

115. (Original) The memory cell according to claim 114, wherein the buffer layer is grown by oxidizing the one electrode.

116. (Previously Presented) A memory cell comprising a capacitor and an access device, wherein the capacitor includes:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer interposed between and directly adjoining the dielectric layer and one of the first and second electrodes, wherein the metal oxide buffer layer includes a refractory metal.

117. (Original) The memory cell according to claim 116, wherein the buffer layer is of the formula MOx, and M is a metal component from a group consisting of tungsten, tantalum, zirconium, and hafnium.

118. (Canceled)

119. (Currently Amended) ~~The~~ A processor and a memory cell ~~according to claim 118,~~ electrically connected to said processor, wherein said memory cell includes a capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode;

a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and one of the first and second electrodes; and

wherein the one electrode is a tungsten nitride and the buffer layer is a tungsten oxide.

120. (Currently Amended) ~~The~~ A processor and a memory cell ~~according to claim 118,~~ electrically connected to said processor, wherein said memory cell includes a capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer intermediate and directly adjoining the dielectric layer and one of the first and second electrodes, wherein the buffer layer has a orthorhombic crystalline structure.

121. (Previously Presented) A processor and a memory cell electrically connected to said processor, wherein said memory cell includes a capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

a tungsten trioxide buffer layer interposed between and directly adjoining the dielectric layer and one of the first and second electrodes.

122. (Original) The memory cell according to claim 121, wherein the one electrode includes tungsten.

123. (Original) The memory cell according to claim 122, wherein the buffer layer is grown by oxidizing the one electrode.

124. (Previously Presented) A processor and a memory cell electrically connected to said processor, wherein said memory cell includes a capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer interposed between and directly adjoining the dielectric layer and one of the first and second electrodes, wherein the metal oxide buffer layer includes a refractory metal.

125. (Original) The memory cell according to claim 124, wherein the buffer layer is of the formula MOx, and M is a metal component from a group consisting of tungsten, tantalum, zirconium, and hafnium.

126. (Canceled)

127. (Currently Amended) The capacitor of claim ~~1~~ 2, wherein the dielectric layer comprises a single layer.